Notice of Allowability	Application No. 09/704,467	Applicant(s) ROTH ET AL.	
	Examiner Aimee J. Li	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *After Final amendments received on 30 October 2007 and 02 November 2007*.

2. ☒ The allowed claim(s) is/are *1, 3, 5-9, 12-16, 19-21, 24-31 renumbered as 1-23*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with John F. Conroy (Reg. No. 45,485) on 20 November 2007.

3. Amendments to the claims are highlighted and strikethrough (~~example~~) or double brackets ([[ex]]) indicates deleted text while underlining (example) indicates added text. The application has been amended as follows:

a. Claim 1 – A method comprising:

i. Receiving a plurality of instructions from a test interface;

ii. Loading the plurality of instructions into an emulation instruction register;

iii. Receiving **[[a]]the** plurality of instructions from the emulation instruction register;

iv. Determining a validity of a first instruction of the plurality of instructions by reading width bits in the first ~~**emulation**~~ instruction, the width bits which are read defining the validity and size of the first ~~**emulation**~~ instruction;

v. Providing the first instruction to a decoder of a processor if the first instruction is valid;

vi. Without receiving a run-test idle state signal, determining a validity of a second instruction of the plurality of instructions by reading width bits in the second instruction, the width bits which are read defining the validity and size of the second ~~emulation~~ instruction; and

vii. Providing the second instruction to the decoder if the second instruction is valid.

b. Claim 15 – The method of Claim 9, ~~further comprising providing the plurality of instructions to~~ **wherein the processor is** a digital signal processor.

c. Claim 16 – A processor comprising:

i. A test interface;

ii. An emulation instruction register adapted to store a plurality of emulation instructions received from the test interface;

iii. Emulation control logic adapted to supply the plurality of emulation instructions to a processor pipeline in response to detection of an entry of the test interface into a run-test idle state, wherein the emulation control logic determines a validity of the plurality of **emulation** instructions by reading bits in each instruction indicating a width of each instruction and discards any invalid instructions; and

iv. A decoder to receive the plurality of **emulation** instructions for processing.

d. Claim 21 – An apparatus, including operating instructions residing on a machine-readable storage medium, for use in a device to handle a plurality of emulation instructions, the operating instructions causing the device to:

i. Load the plurality of emulation instructions into a single emulation instruction register;

ii. Have a test interface enter a run-test idle state;

iii. Provide the plurality of emulation instructions to a processor in response to entry of the test interface into the run-test idle state; and

iv. Process the plurality of emulation instructions,

v. Wherein a validity of each of the plurality of **emulation** instructions is determined before processing by reading bits in each instruction indicating a width of each **emulation** instruction.

e. Claim 28 – The processor of Claim 16,further comprises a multiplexer to select ~~**between**~~ an instruction ~~**for**~~ **from** the plurality of **emulation** instructions to send to the processor pipeline.

Reasons for Allowance

4. The following is an examiner's statement of reasons for allowance: As stated in previous Office Actions dated 08 March 2007 and 22 August 2007, the claims contain the limitations, taking claim 1 as exemplary, "determining a validity of a first instruction of the plurality of instructions by reading width bits in the first instruction, the width bits which are read defining the validity and size of the first instruction". None of the prior art searched and found has taught this limitation in combination with other limitations in the claims. The prior art searched and

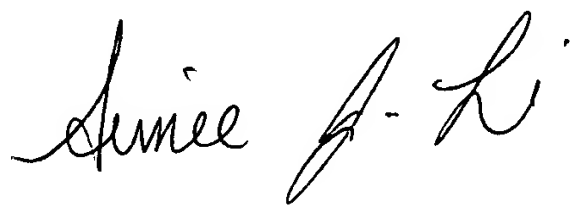
found has taught determining the validity of an instruction of each of the plurality of instructions before processing, but not that the validity was determined based upon the width bits inside of the instruction. Other prior art searched and found taught that width bits inside of the instruction exist, but not that they would be used to define and determine the validity of an instruction. Neither of these types of prior art taught that determining the validity of an instruction nor the instructions contain width bits in test interfaces. The prior art also did not suggest or provide a motivation obvious to a person of ordinary skill in the art to combine all the separate references, since most test interfaces are developed under the assumption that they will be written to be automatically compatible with the system.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

7. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Aimee J Li
Examiner
Art Unit 2183

21 November 2007